

CLAIMS

What is claimed is:

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1. A method for scheduling tasks in a wafer processing system comprising:
defining a plurality of operations that can be run on said wafer processing system;
adding at least one of said plurality of operations to an operation list;
switching an operation in said operation list to an active state; and
scheduling all operations in said operation list that are in the active state to run on said wafer processing system.
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2. The method of claim 1 wherein each of said plurality of operations includes conditions for adding an operation to said operation list.
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3. The method of claim 1 wherein each of said plurality of operations includes conditions for switching an operation in the operation list to an active state.
4. The method of claim 1 wherein said plurality of operations includes a recipe operation.
5. The method of claim 1 wherein said plurality of operations includes a recipe operation and a non-recipe operation.
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6. A wafer processing system including a computer, said computer having a computer readable storage memory containing a plurality of operations that can be run on said wafer processing system, said computer readable storage memory further containing instructions for (a) adding at least one of said plurality of operations to an operation list, (b) switching an operation in said operation list to an active state, and (c) scheduling all operations in said operation list that are in the active state to run.

7. The wafer processing system of claim 6 wherein each of said plurality of operations includes conditions for adding an operation to said operation list.

8. The wafer processing system of claim 6 wherein each of said plurality of operations includes conditions for switching an operation in the operation list to an active state.

9. The wafer processing system of claim 6 wherein at least one of said plurality of operations is a recipe operation.

10. A data structure for an operation to be performed on a wafer processing system comprising:

a first level including conditions for adding said operation to an operation list and conditions for switching said operation to an active state; and

a second level including a sequence of actions to be performed on said wafer processing system.

11. The data structure of claim 10 wherein said first level further includes a list of modules to be used by said operation.

12. The data structure of claim 10 wherein said operation is a recipe operation.

13. The data structure of claim 12 wherein said second level further includes a list of wafers to be processed in accordance with said recipe operation.